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DATA SHEET

TEA0679T

I²C-bus controlled dual Dolby* B-type noise reduction circuit for playback applications

Product specification
Supersedes data of 1998 Jun 24
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Philips Semiconductors

PHILIPS

I²C-bus controlled dual Dolby* B-type noise reduction circuit for playback applications

TEA0679T

FEATURES

- Dual Noise Reduction (NR) channels
- Head preamplifiers
- Reverse head switching
- Automatic Music Search (AMS)
- Blank skip
- Mute position
- Equalization with electronically switched time constants
- Switch functions and level adjustment controlled via I²C-bus
- Optional switch inputs TTL compatible
- Dolby reference level = 387.5 mV
- Contained in a 32-pin small outline package
- Improved EMC behaviour.

GENERAL DESCRIPTION

The TEA0679T is a bipolar integrated circuit that provides two channels of Dolby B noise reduction for playback applications in car radios. It includes head and equalization amplifiers with electronically switchable time constants. The device also includes electronically switchable inputs for tape drivers with reverse heads.

This device detects pauses of music in the Automatic Music Search (AMS) scan mode (for applications with an intelligent controlled tape driver) or AMS latch mode (for applications with a simple controlled tape driver).

For both modes the delay time can be fixed by using an external resistor. In the blank skip mode the IC can detect pauses of music during playback and allows a microcontroller to react on this situation.

The equalization amplifier gain adjustment, the output offset adjustment and all switching functions are I²C-bus controlled. Head switching and equalization time constant switching can be controlled via separate pins (optional). The device operates with power supplies from 7.6 to 12 V. The output overload level increases with increases in supply voltage.

Current drain varies with the following variables:

- Supply voltage
- Noise reduction on/off
- AMS on/off.

Because of this current drain variation it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.6	–	12	V
I_{CC}	supply current	–	35	40	mA
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	78	84	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA0679T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

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TEA0679T

BLOCK DIAGRAM

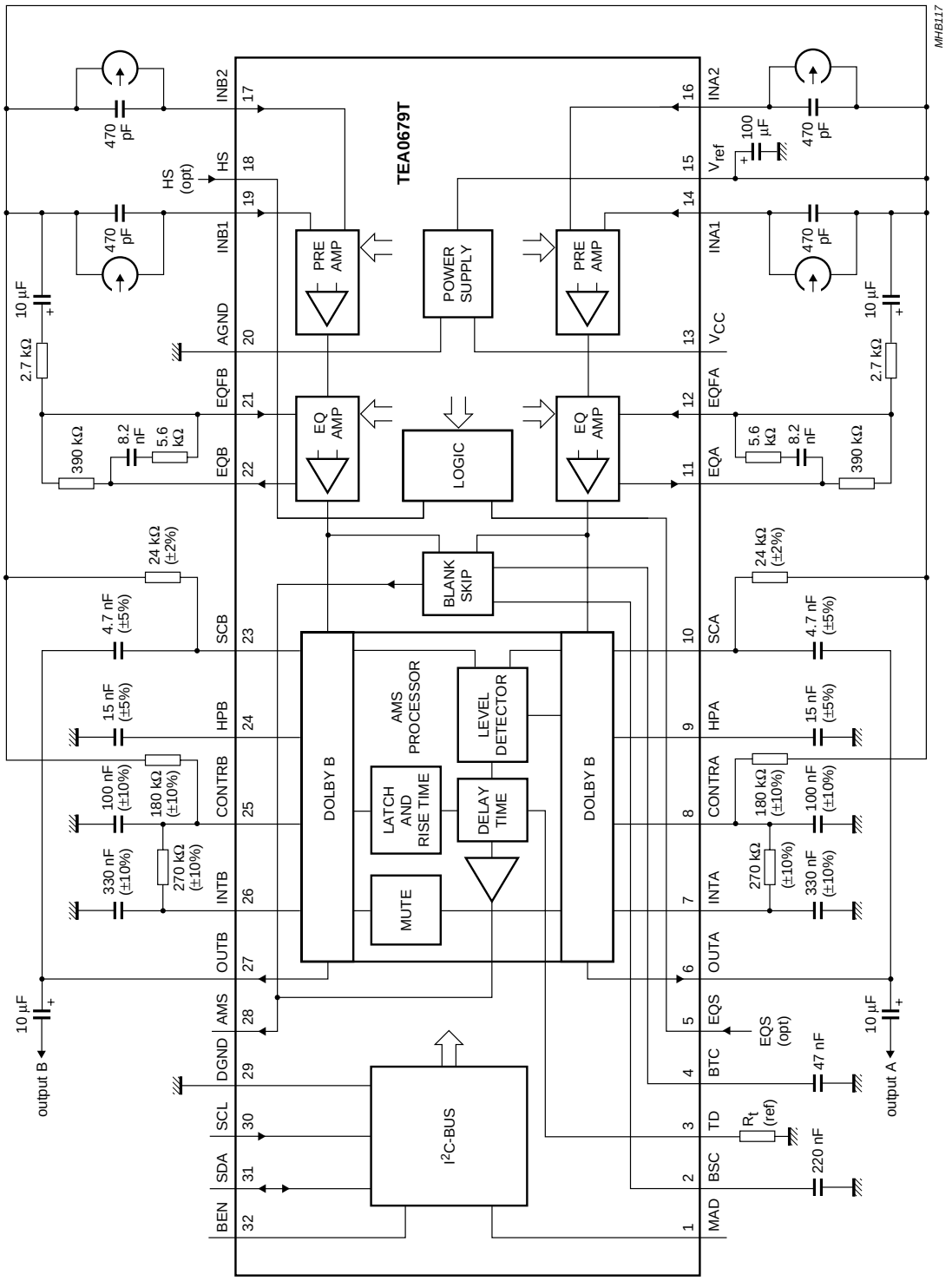


Fig.1 Block and application diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MAD	1	programmable address bit
BSC	2	blank skip reference capacitance
TD	3	delay time constant
BTC	4	blank skip integration capacitance
EQS	5	equalization switch input (optional)
OUTA	6	output channel A
INTA	7	integrating filter channel A
CONTRA	8	control voltage channel A
HPA	9	high-pass filter channel A
SCA	10	side chain channel A
EQA	11	equalizing output channel A
EQFA	12	equalizing input channel A
V_{CC}	13	supply voltage
INA1	14	input channel A1 (forward or reverse)
V_{ref}	15	reference voltage
INA2	16	input channel A2 (reverse or forward)
INB2	17	input channel B2 (reverse or forward)
HS	18	head switch input (optional)
INB1	19	input channel B1 (forward or reverse)
AGND	20	analog ground
EQFB	21	equalizing input channel B
EQB	22	equalizing output channel B
SCB	23	side chain channel B
HPB	24	high-pass filter channel B
CONTRB	25	control voltage channel B
INTB	26	integrating filter channel B
OUTB	27	output channel B
AMS	28	Automatic Music Search (AMS) output
DGND	29	digital ground
SCL	30	serial clock input
SDA	31	serial data input/output
BEN	32	bus enable

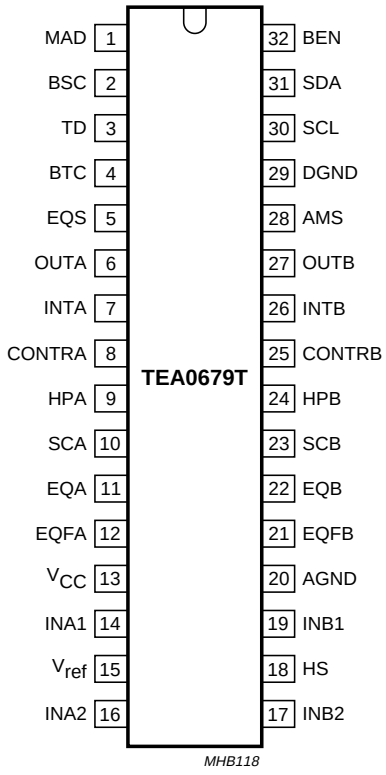


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The following functions can be controlled via the I²C-bus:

- Equalization time constant switching
- Head switching
- Automatic Music Search (AMS) modes and blank skip
- Noise Reduction (NR) on/off switching
- Mute switching
- Equalization amplifier gain adjustment
- Output offset adjustment.

Dolby B noise reduction only operates correctly if the 0 dB Dolby level is adjusted at 387.5 mV. The gain adjustment can also be used to change the AMS level detector threshold. The IC is able to generate an internal power-on reset to guarantee a proper start-up behaviour.

Two of the above functions can be controlled via separate pins (optional), if required.

Head switching is achieved when pin HS is connected to a LOW level (input IN2 active) or connected to a HIGH level (input IN1 active).

Equalization time constant switching (70 or 120 μs) is achieved when pin EQS is connected to a LOW level (70 μs) or connected to a HIGH level (120 μs).

If I²C-bus control is used the respective external function control pin has to be left open-circuit. When open-circuit the current state of the function can be observed at these pins.

Automatic Music Search (AMS) modes and blank skip

If AMS is active (search mode bits SMOD1 = 1 and SMOD0 = 0 or 1) the NR function is internally switched off and the equalization time constant is internally forced to 70 μs. The signals of both channels are full-wave rectified and then added. This means that even if one channel appears inverted to the other channel the normal AMS function is ensured.

It is possible to choose between the AMS scan and the AMS latch mode via the I²C-bus. Due to the usage of an internal flip-flop the switching from one mode to the other must be done via the AMS off state. This guarantees an appropriate flip-flop reset:

- Start from the initial AMS off state (SMOD1 = 0 and SMOD0 = 0 or 1)
- Enable the desired AMS operation mode: AMS latch mode (SMOD1 = 1 and SMOD0 = 0) or AMS scan mode (SMOD1 = 1 and SMOD0 = 1).

For further information on music search see Figs 4 to 8.

If blank skip is active (SMOD1 = 0 and SMOD0 = 1) periods of music can be detected in the playback mode using the AMS pin as the detector output. It is possible to defeat this function via the I²C-bus (SMOD1 = 0 and SMOD0 = 0). For further information on blank skip see Figs 9 and 10.

Offset adjustment procedure

The offset adjustment is performed using two bits in the I²C-bus write byte 0. The offset monitor bit OMOR enables the AMS output to indicate whether the selected offset value is positive or negative. The channel select bit OFCH selects the channel (A or B) which is currently monitored by the output at pin AMS. The monitoring needs a few microseconds until the output result is valid. A complete offset adjustment is performed in the following way:

- Adjust the output to Dolby level using the I²C-bus controlled equalization gain adjustment
- Enable the offset monitor and select the channel to be monitored by transmitting the bits OMOR = 1 and OFCH (0 = Channel A, 1 = Channel B) to the IC
- If the monitor output (pin AMS) is LOW send the next offset value OFFCHA or OFFCHB one offset step below the last valid value. If the monitor output (pin AMS) is HIGH send the next offset value OFFCHA or OFFCHB one offset step above the last valid value
- Repeat the last two steps until the monitor output changes its polarity
- If necessary store the transmitted digital offset value for the selected channel.

The start value is either set by the power-on reset or the last I²C-bus transmission. The offset adjustment can be performed during the power-on reset condition and also each time the tape driver is not active. A complete digital offset data set consists of four values: one for each head (head 1 and head 2) in each channel. After an offset value transmission the IC stores one value for channel A and one value for channel B. If a head switch is performed these values have to be updated via the I²C-bus for the alternative head.

I²C-bus operation mode

The IC is capable of operating with I²C-bus systems that provide either 5 V or digital supply voltage related logic levels below 5 V. This is achieved using the bus enable (pin 32) with different input voltages. An open pin or input voltages above 5 V enable 5 V related I²C-bus logic levels. If input voltages between 3 and 5 V are used the IC operates with I²C-bus logic levels related to these input voltages. To disable the I²C-bus receiver it is necessary to use pin voltages below the specified LOW level.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	14	V
V_i	input voltage (pins 1 to 32) except pin 5 (EQS), pin 15 (V_{ref}), pin 18 (HS), pin 30 (SCL) and pin 31 (SDA) to V_{CC}		–0.3	V_{CC}	V
$V_{i(n1)}$	input voltage at pin 30 (SCL) and pin 31 (SDA)		–0.3	+12	V
$V_{i(n2)}$	input voltage at pin 5 (EQS) and pin 18 (HS)		–0.3	+6.5	V
$V_{i(stb)}$	standby input voltage at pin 1 (MAD), pin 32 (BEN), pin 5 (EQS) and pin 18 (HS)	note 1	–0.3	+6.5	V
t_{sc}	pin 15 (V_{ref}) to V_{CC} short-circuiting duration		–	5	s
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage for all pins	note 2	–2	+2	kV
		note 3	–500	+500	V

Notes

1. The TEA0679T allows a HIGH level at switching pins without voltage (V_{CC} = 0; standby mode). This means a maximum input voltage of 6.5 V for the switching pins.
2. Human body model (1.5 kΩ; 100 pF).
3. Machine model (0 Ω; 200 pF).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	62	K/W

CHARACTERISTICS

V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = 25 °C; all levels are referenced to V_o = 387.5 mV (RMS) (0 dB) at test point (TP) pin OUTA or OUTB; see Fig.1; NR on/AMS off; EQ switch in the 70 µs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.6	10	12	V
I_{CC}	supply current		–	35	40	mA
α_m	channel matching	f = 1 kHz; V_o = 0 dB; NR off	–0.5	–	+0.5	dB
THD	total harmonic distortion (2nd and 3rd harmonic)	f = 1 kHz; V_o = 0 dB	–	0.08	0.15	%
		f = 10 kHz; V_o = 10 dB	–	0.15	0.3	%
H_R	headroom at output	V_{CC} = 7.6 V; THD = 1%; f = 1 kHz	12	–	–	dB
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	internal gain 40 dB, linear; CCIR/ARM weighted; decode mode; see Fig.41	78	84	–	dB
PSRR	power supply ripple rejection	$V_{i(rms)}$ = 0.25 V; f = 1 kHz; see Fig.38	52	57	–	dB
V_o	output voltage frequency response; referenced to TP	encode mode; see Fig.41				
		–25 dB; f = 0.2 kHz	–25.9	–24.4	–22.9	dB
		0 dB; f = 1 kHz	–1.5	0	+1.5	dB
		–25 dB; f = 1 kHz	–20.8	–19.3	–17.8	dB
		–25 dB; f = 5 kHz	–21.1	–19.6	–18.1	dB
		–35 dB; f = 10 kHz	–27.4	–25.9	–24.4	dB
α_{cs}	channel separation	V_o = 10 dB; f = 1 kHz; see Fig.39	57	63	–	dB
α_{ct}	crosstalk between active and inactive input	f = 1 kHz; V_o = 10 dB; NR off; see Fig.39	70	77	–	dB
R_L	load resistance at output	AC-coupled; f = 1 kHz; V_o = 12 dB; THD = 1%	10	–	–	kΩ
G_v	voltage gain of preamplifier	pin INA1/INA2 to pin EQFA; pin INB1/INB2 to pin EQFB; f = 1 kHz	29	30	31	dB
$V_{i(offset)(DC)}$	DC input offset voltage		–	2	–	mV
$I_{i(bias)}$	input bias current		–	0.1	0.4	µA
R_{EQ}	internal equalization resistor	pin EQA/EQB to EQ amplifier A/B output	4.7	5.8	6.9	kΩ
R_i	input resistance of head inputs		60	100	–	kΩ
$G_{v(ol)}$	open-loop gain	pin INA1 or INA2 to pin EQA; pin INB1 or INB2 to pin EQB; additional gain = 0 dB				
		f = 10 kHz	80	86	–	dB
		f = 400 Hz	104	110	–	dB
$V_{ref} - V_{OUT}$	DC output offset voltage at pins OUTA and OUTB after adjustment	NR off; pins INA1, INA2, INB1 and INB2 connected to V_{ref}	–20	–	+20	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_O	DC output current	pins OUTA and OUTB connected to ground	–2	–	–	mA
		pins OUTA and OUTB connected to V_{CC}	0.3	–	–	mA
Z_o	output impedance		–	80	100	Ω
$V_{no(rms)}$	equivalent input noise voltage (RMS value)	NR off; unweighted; f = 20 Hz to 20 kHz; R_{source} = 0 Ω	–	0.7	1.4	μV
V_{TD}	AMS timing (DC level)	resistor R_t connected to pin TD	V_{CC} – 3	–	V_{CC}	V
$V_{offset(DC)}$	DC offset voltage at pins OUTA and OUTB	f = 900 MHz; $V_{i(rms)}$ = 6 V	–	40	–	mV
$V_{offset(AD)}$	overall offset voltage between AGND (pin 20) and DGND (pin 29)		–0.4	–	+0.4	V
Level adjustment						
G_{CR}	gain control range	note 1	24.2	25.2	26.2	dB
G_{step}	step size		–	0.4	–	dB
G_E	step error between any adjacent step		–	–	0.4	dB
Switching thresholds						
OPTIONAL EQUALIZATION TIME CONSTANT SWITCH (pin EQS)						
V_{IL}	LOW-level input voltage	70 μs; $I_L \geq -200$ μA	–0.3	–	+0.8	V
V_{OL}	LOW-level output voltage	70 μs; $I_L \leq 1$ mA	–	–	0.4	V
V_{IH}	HIGH-level input voltage	120 μs	2	–	–	V
V_{OH}	HIGH-level output voltage	120 μs; $I_L \geq -50$ μA	2.8	–	3.3	V
OPTIONAL HEAD SWITCH (pin HS)						
V_{IL}	LOW-level input voltage	INPUT 2 on; $I_L \geq -150$ μA	–0.3	–	+0.8	V
V_{OL}	LOW-level output voltage	INPUT 2 on; $I_L \leq 10$ μA	–	–	0.4	V
V_{IH}	HIGH-level input voltage	INPUT 1 on	2	–	–	V
V_{OH}	HIGH-level output voltage	INPUT 1 on; $I_L \geq -50$ μA	2.8	–	3.3	V
Search modes						
BLANK SKIP						
$BS_{th(M-P)}$	dynamic level threshold	blank skip mode; f = 10 kHz	–30	–27	–24	dB
$t_{sw(P-M)}$	switching time pause-to-music	blank skip mode; f = 10 kHz; signal on channel A and B; note 2	2.1	4.15	6.3	ms
		blank skip mode; f = 10 kHz; signal on one channel; note 2	4.1	8.3	12.5	ms
$t_{sw(M-P)}$	switching time music-to-pause	blank skip mode; f = 10 kHz; note 2	10	19	30	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AUTOMATIC MUSIC SEARCH (AMS)						
$t_{W(min)(r)}$	minimum pulse width rise time	AMS scan mode	2	–	10	ms
		AMS latch mode	130	–	170	ms
$AMS_{(P-M)}$	signal level at output for AMS switching pause-to-music	AMS mode; f = 10 kHz; notes 3 and 4; see Fig.40	–23.7	–21	–18	dB
$AMS_{(M-P)}$	AMS switching hysteresis music-to-pause	AMS mode; f = 10 kHz	–0.7	–1	–1.3	dB
OUTPUT (pin AMS)						
V_{OH}	HIGH-level output voltage	$I_L \geq -1$ mA	2.8	–	3.3	V
V_{OL}	LOW-level output voltage	$I_L \leq 1$ mA	–	–	0.4	V
Digital part (pins MAD and BEN)						
V_{IH}	HIGH-level input voltage		3	–	V_{CC}	V
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH-level input current		–10	–	+10	µA
I_{IL}	LOW-level input current		–10	–	+10	µA
Digital part (pins SDA and SCL); note 4						
V_{IH}	HIGH-level input voltage	BEN (pin 32) open-circuit	3	–	V_{CC}	V
		$5 V \leq V_{BEN} \leq V_{CC}$	3	–	V_{CC}	V
		$3 V \leq V_{BEN} < 5 V$	$0.7V_{BEN}$	–	V_{CC}	V
V_{IL}	LOW-level input voltage	BEN (pin 32) open-circuit	–0.3	–	+1.5	V
		$5 V \leq V_{BEN} \leq V_{CC}$	–0.3	–	+1.5	V
		$3 V \leq V_{BEN} < 5 V$	–0.3	–	$0.3V_{BEN}$	V
I_{IH}	HIGH-level input current	V_{CC} = 0 to 12 V	–10	–	+10	µA
I_{IL}	LOW-level input current		–10	–	+10	µA
V_{OL}	LOW-level output voltage SDA	I_L = 3 mA	–	–	0.4	V

Notes

1. For Dolby NR level adjust and AMS pause detection level setting.
2. All blank skip timing characteristics are based on the assumption that a signal level change from –33 to –21 dB pause-to-music or –21 to –33 dB music-to-pause occurs in the specified channels.
3. The high speed of the tape (FF and REW) at the tape head during AMS mode causes a transformation of level and frequency of the originally recorded signal. It means a boost of signal level of approximately 10 dB and more for recorded frequencies from 500 Hz to 4 kHz. So the threshold level of –22 dB corresponds to signal levels in PlayBack (PB) mode of approximately –32 dB. The AMS inputs for each channel are pins SCA and SCB. As the frequency spectrum is transformed by a factor of approximately 10 to 30 due to the higher tape speed in FF and REW, the high-pass filter (4.7 nF/24 kΩ) removes the effect of offset voltages but does not affect the music search function. In the block and application diagram (see Fig.1) the frequency response of the system between tape heads input, e.g. pins INA2 and INB2, to the AMS input pins SCA and SCB is constant over the whole frequency range (see Fig.3).
4. These levels correspond to a gain setting of Dolby level at TP (for TP see Fig.41). The gain adjustment can be used to change the threshold level during AMS operation.
5. The characteristics are in accordance with the I²C-bus specification. Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011).

General note

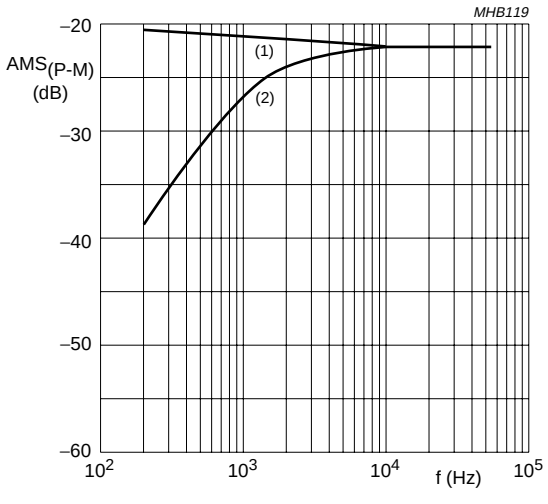
It is recommended to switch off V_{CC} with a gradient of 400 V/s at maximum to avoid plops on tape in the event of contact between tape and tape head while switching off.

AMS delay time

Table 1 AMS delay time set by resistor R_t at pin TD

RESISTOR VALUE R_t (kΩ)	DELAY TIME t_d TYP. (ms)	TOLERANCE (%)
68	23	20
150	42	15
180	48	15
220	56	15
270	65	10
330	76	10
470	98	10
560	112	10
680	126	10
820	142	10
1000	160	10

AMS threshold level



(1) AMS threshold level for application circuit (see Fig.1).
(2) AMS threshold level for test circuit (see Fig.40).

Fig.3 AMS threshold level.

Short description of music search

A system for music search consists mainly of a level and a time detection circuit (see Fig.4). For adapting and decoupling the input signal is amplified (A), then rectified (B) and smoothed with a time constant (C). Thus the voltage at (C) corresponds to the signal level and will be compared to the predefined pause level at the first comparator (D), the level detector. If the signal level becomes smaller than the pause level, the level detector changes its output signal. Due to the output level of the level detector the capacitor of the second time constant (E) will be charged, respectively discharged.

If the pause level of the input signal remains for a certain time period, the voltage at the capacitor reaches a certain value, which corresponds to an equivalent time value. The voltage at the capacitor will be compared to a predefined time-equivalent voltage by the second comparator (F), the time detector. If the pause level of the input signal remains for this predefined time, the time detector changes its output level to pause found status.

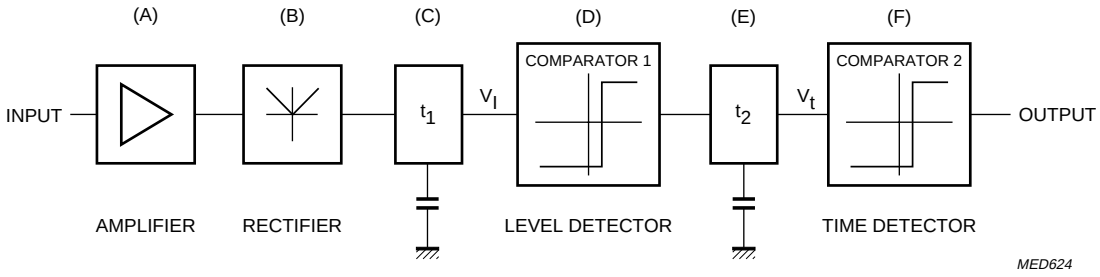


Fig.4 Integrated music search function.

Description of the principle timing diagram for AMS scan mode without initial input signal (see Fig.5)

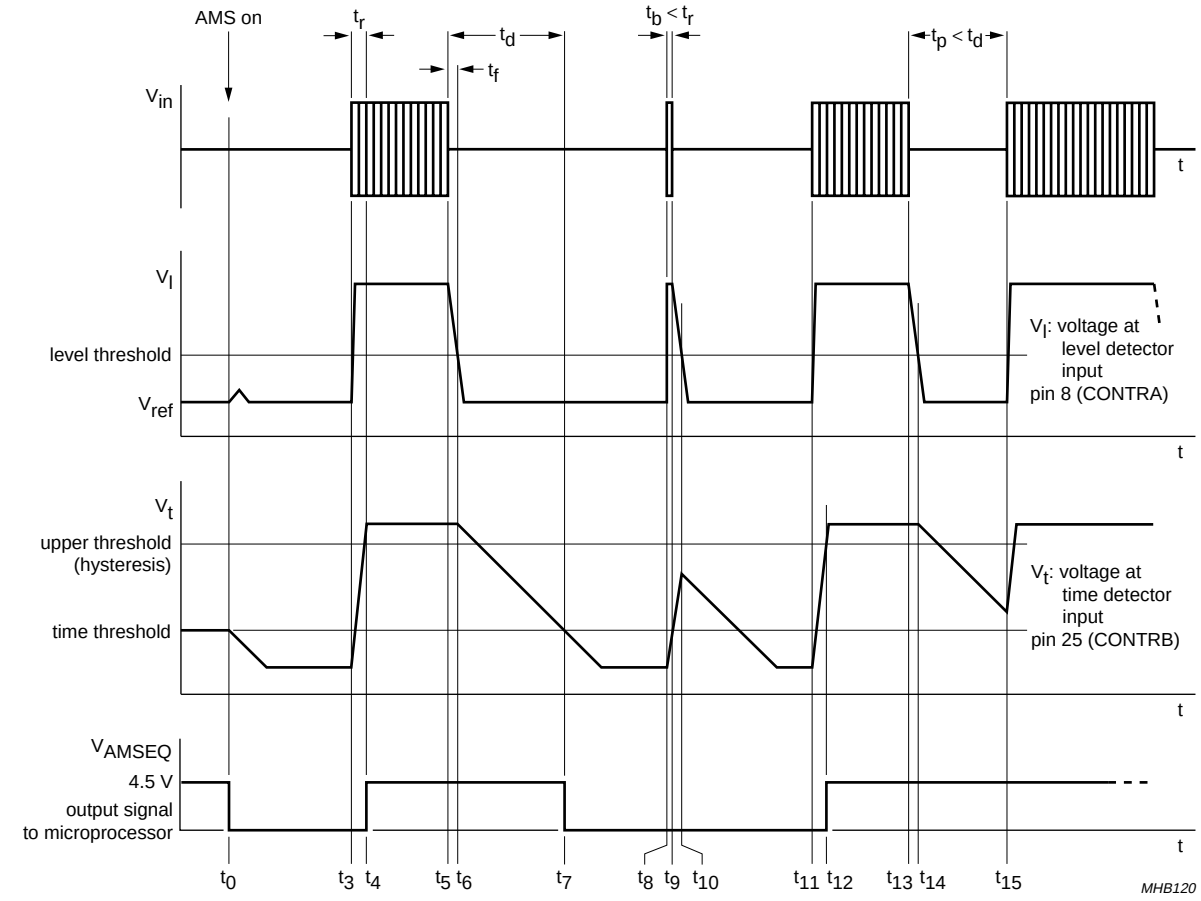
By activating the AMS scan mode the AMS output level directly indicates whether the input level corresponds to a pause level (V_{AMSEQ} = LOW) or not (V_{AMSEQ} = HIGH). At t_0 the AMS scan mode is activated. Without a signal at V_{in}, the following initial procedure runs until the AMS output changes to a LOW level: due to no signal at V_{in} the voltage at the level detector input V_l (CONTRA) remains below the level threshold and the second time constant will be discharged (time detector input V_t). When V_t exceeds the time threshold level, the time detector output changes to LOW level. Now the initial procedure is completed.

If a signal burst appears at t_3, the level detector input voltage rises immediately and causes its output to charge the second time constant, which supplies the input voltage V_t for the time detector.

When V_t exceeds the upper threshold level after the rise time t_r (at t_4) the AMS output changes to HIGH. If the signal burst ends at t_5 the level detector input V_l falls to its LOW level. Discharging of the second time constant begins when the level threshold is exceeded at t_6. The circuit then measures the delay time t_d, which is externally fixed by a resistor and defines the length of a pause to be detected. If no signal appears at V_{in} within the time interval t_d, the time detector output switches the AMS output to a LOW level at t_7.

If a plop noise pulse appears at V_{in} (t_8) with a pulse width less than the rise time $t_r > t_b$, the plop noise will not be detected as music. The AMS output remains LOW.

Similarly the system handles no music pulses t_p: when music appears at t_{11} with a small interruption at t_{13}, this interruption will not affect the AMS output for $t_p < t_d$.



t_r = rise time; t_d = delay time; t_b = burst time; t_p = pause time; t_f = fall time.

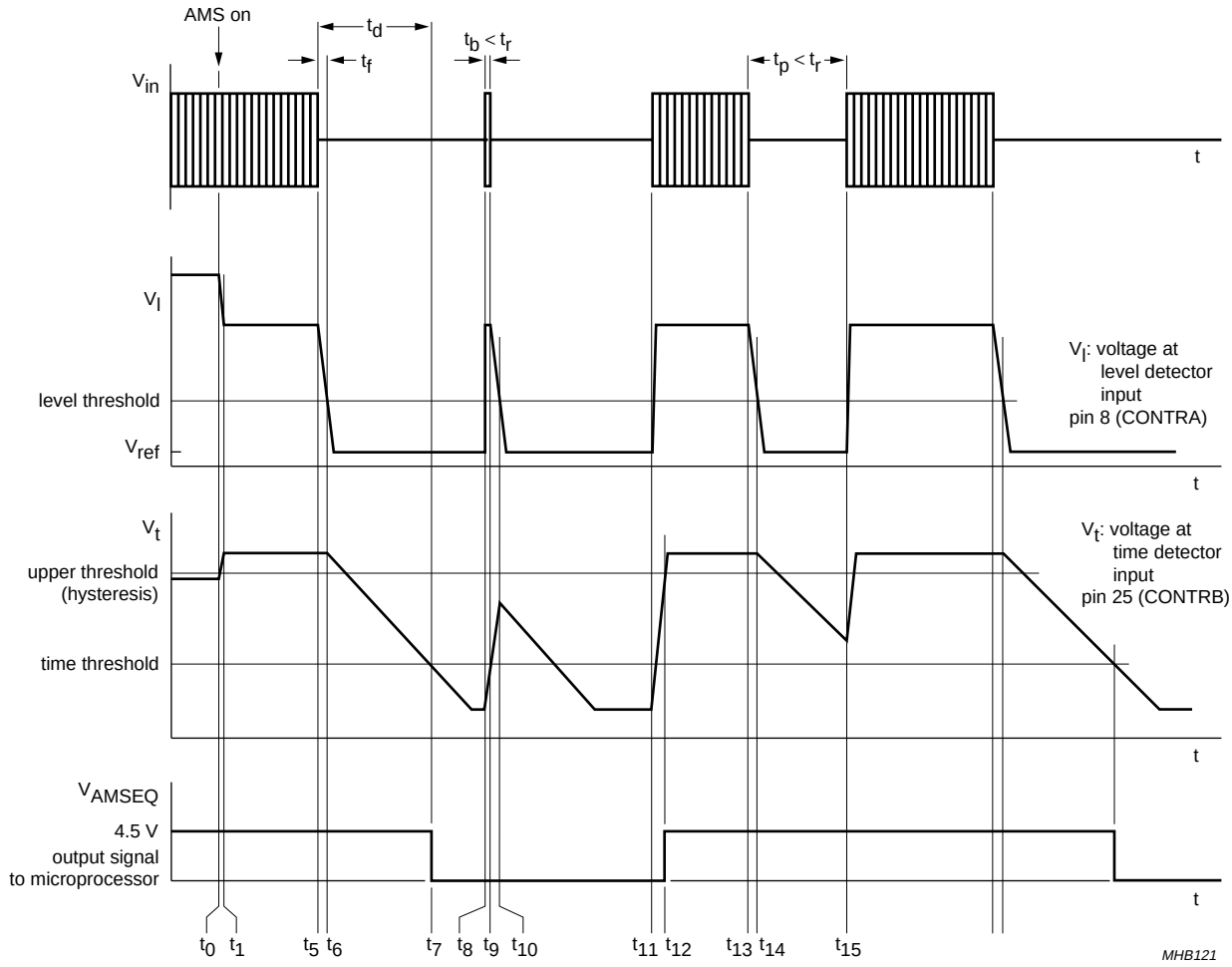
Fig.5 AMS scan mode without initial input signal.

Description of the principle timing diagram for AMS scan mode with initial input signal (see Fig.6)

The AMS scan mode is activated at t_0. With an input signal at V_{in}, the following initial procedure runs until the circuit gets a steady state status.

Due to the signal at V_{in} the voltage at the level detector input V_l (CONTRA) slides to a value which is defined by a limiter. This voltage causes the level detector output to charge the second time constant (time detector input V_t) to its maximum voltage level at t_1. The initial procedure is now completed.

The following behaviour does not differ from the description in Section “Description of the principle timing diagram for AMS scan mode without initial input signal (see Fig.5)”.



t_r = rise time; t_d = delay time; t_b = burst time; t_p = pause time; t_f = fall time.

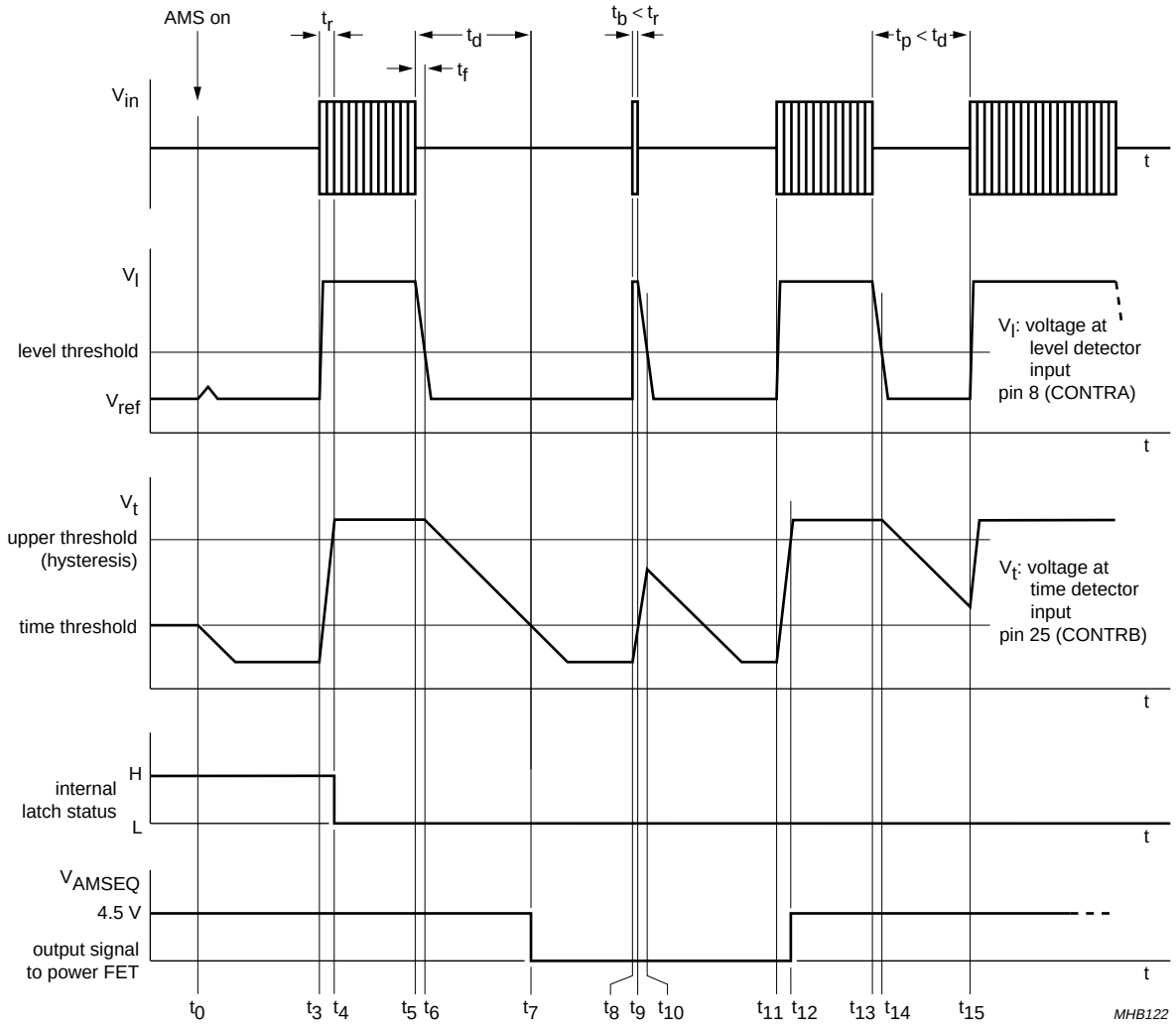
Fig.6 AMS scan mode with initial input signal.

Description of the principle timing diagram for AMS latch mode without initial input signal (see Fig.7)

This is similar to the description of the principle timing diagram from AMS scan mode. It only differs in its initial behaviour and its rise time t_r (it should be noted that the different t_r does not occur in the principle timing diagrams for latch and scan mode).

Running in AMS latch mode, the circuit may be simply applied to drive a stop solenoid via a power FET. So a further processing of the AMS output signal is not necessary. Because there is no processor to make a decision whether there is plop noise or not, for this mode the rise time t_r is extended to approximately 150 ms.

By activating the AMS latch mode the AMS output will not change to a LOW level at t_0 if there is no initial signal at V_{in}. A latch forces the AMS output to remain HIGH until a signal appears at V_{in} (t_4). After t_4 the latch will not affect the output until the AMS latch mode is started again.
The existence of the latch appears necessary if the AMS output, for example, drives a stop solenoid via a power FET. The LOW output level will cause a drive of the stop solenoid. This will happen after a maximum time of t_d occurs without any input signal. If there is no music on tape for a long time (e.g. at tape end), the AMS mode will be activated repeatedly as long as there is no signal at V_{in}. Thus the circuit waits until music appears before detecting the pauses.



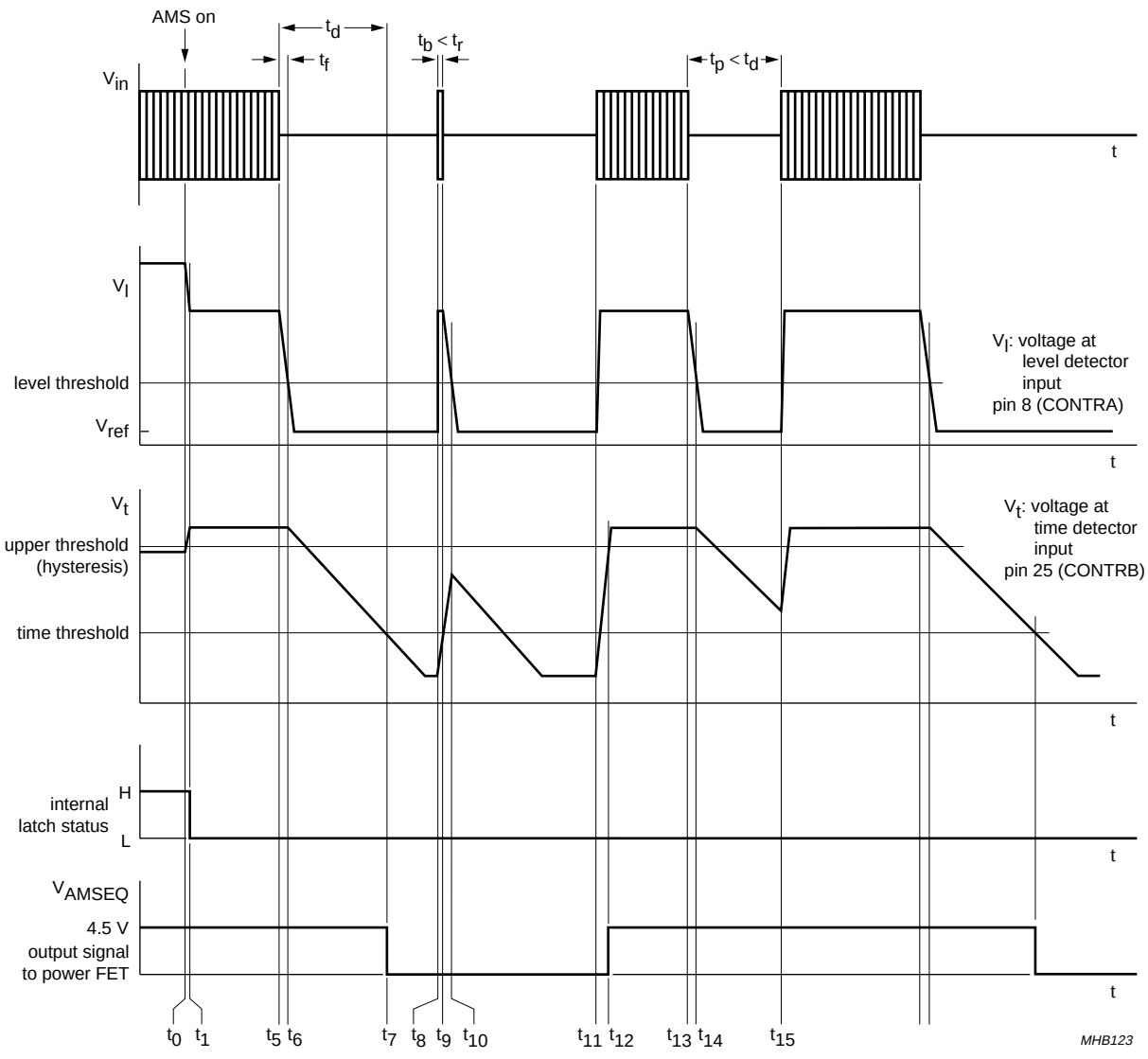
t_r = rise time; t_d = delay time; t_b = burst time; t_p = pause time; t_f = fall time.

Fig.7 AMS latch mode without initial input signal.

Description of the principle timing diagram for AMS latch mode with initial input signal (see Fig.8)

This is similar to the description in Section “Description of the principle timing diagram for AMS scan mode with initial input signal (see Fig.6)”. It only differs in its rise time t_r and a release of its internal latch when voltage V_t exceeds the upper threshold between t_0 and t_1. The initial procedure is now completed.

The following behaviour does not differ from the description in Section “Description of the principle timing diagram for AMS latch mode without initial input signal (see Fig.7)”.



t_r = rise time; t_d = delay time; t_b = burst time; t_p = pause time; t_f = fall time.

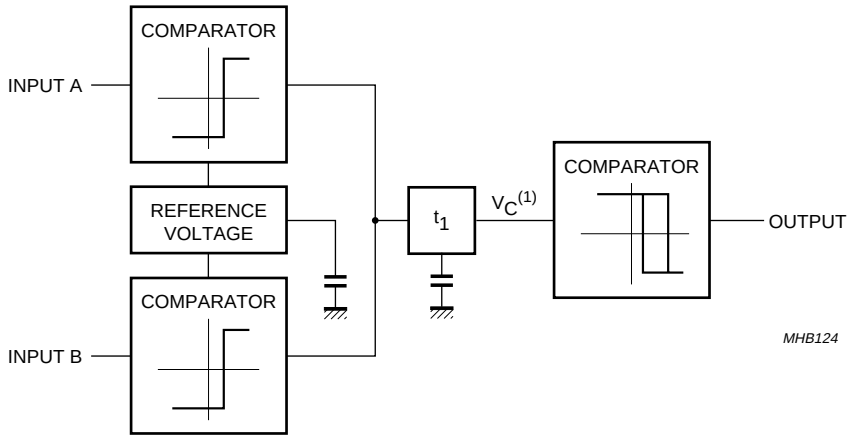
Fig.8 AMS latch mode with initial input signal.

Short description of blank skip

The blank skip system is intended to detect pauses of music during playback mode. It consists of two input signal level comparators, an integration capacitor and an output comparator with hysteresis. The DC voltage of the inputs A and B, increased by the level threshold value, is used as the reference voltage for the input comparators. If input A or B exceeds this voltage the integration capacitor is discharged. If this voltage falls below the lower threshold the output comparator changes its polarity to the music found status.

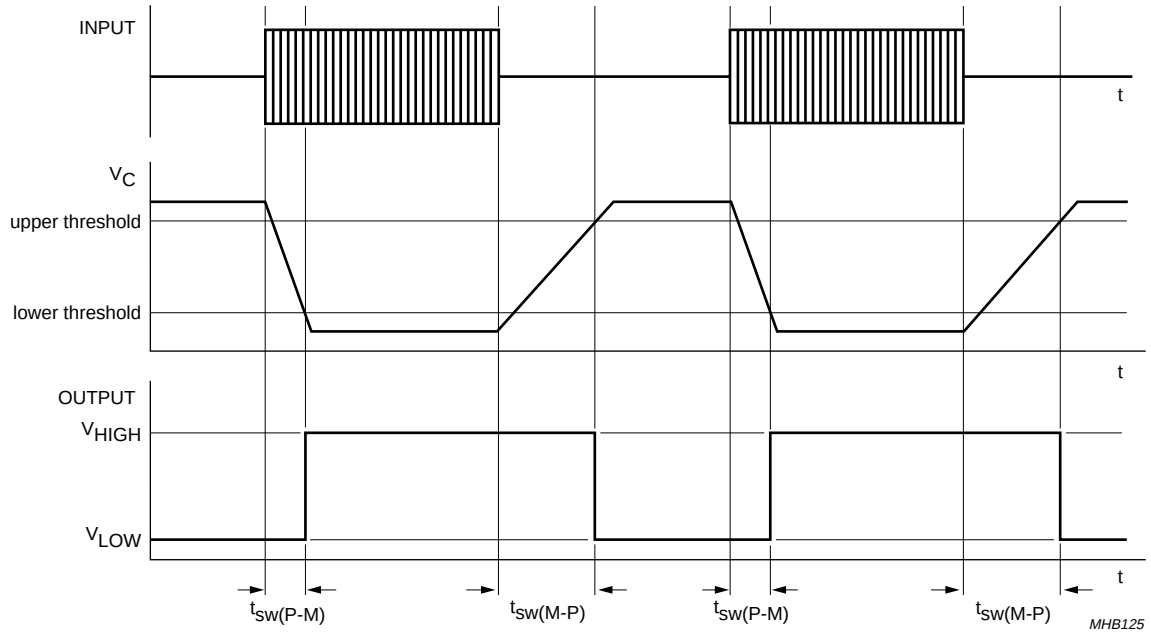
In the event that none of the two inputs A or B exceeds the level threshold the integration capacitor is charged. After its voltage has exceeded the upper threshold of the output comparator the output changes its polarity to the pause found status.

It is recommended to process the output signal with a microcontroller to perform, for example, spike suppression for a certain time.



(1) V_C: integration capacitor voltage.

Fig.9 Integrated blank skip function.



V_C; integration capacitor voltage: $t_{sw(P-M)}$; switching time pause-to-music: $t_{sw(M-P)}$; switching time music-to-pause.

Fig.10 Blank skip timing diagram.

Soft head switching

In general the head switching procedure is recommended to be performed in four steps:

1. Activate the mute function
2. Switch to the alternative head
3. Adjust the offset for the new head
4. Deactivate the mute function.

In applications without a mute function a soft head switch via the I²C-bus can be realized using a capacitor connected to pin 18. A proposal for this switching mechanism is shown in Fig.11. To guarantee the internal timing for the head switching operation an externally connected device to pin 18 should not modify the output current significantly.

An additional resistor is necessary if the head switching is performed externally via the optional switching input capability at pin 18. A proposal for this kind of switching is shown in Fig.12.

In general soft head switching is only suitable if equal offset values for head 1 and head 2 exist. A soft offset value switching is not possible with the TEA0679T.

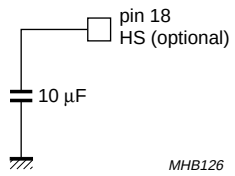


Fig.11 Soft head switching via the I²C-bus.

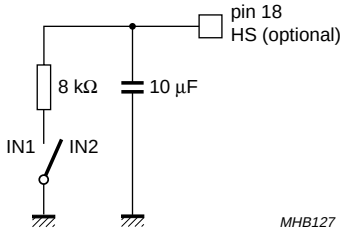


Fig.12 External soft head switching.

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	DATA	A	P

Table 2 Explanation of I²C-bus format to read (slave transmits data)

NAME	DESCRIPTION
S	START condition
SLAVE ADDRESS	101 100 00 (MAD = LOW) 101 100 10 (MAD = HIGH)
A	acknowledge; generated by the slave
DATA	see Tables 3 to 10
P	STOP condition

Table 3 Write byte 0; SELECT

FUNCTIONS	BITS OF DATA BYTE SELECT							
	MSB							LSB
	SMOD1	SMOD0	HSW	MUTE	NROF	OFCH	OMOR	EQT
Equalization time constant								
70 µs	–	–	–	–	–	–	–	0
120 µs	–	–	–	–	–	–	–	1
Offset monitor								
AMS output	–	–	–	–	–	–	0	–
offset monitor	–	–	–	–	–	–	1	–
Offset channel								
channel A	–	–	–	–	–	0	–	–
channel B	–	–	–	–	–	1	–	–
NR on/off								
on	–	–	–	–	0	–	–	–
off	–	–	–	–	1	–	–	–
Mute off/on								
off	–	–	–	0	–	–	–	–
on	–	–	–	1	–	–	–	–
Head switch								
IN2	–	–	0	–	–	–	–	–
IN1	–	–	1	–	–	–	–	–
Search mode								
off	0	0	–	–	–	–	–	–
blank skip	0	1	–	–	–	–	–	–
AMS latch mode	1	0	–	–	–	–	–	–
AMS scan mode	1	1	–	–	–	–	–	–

Table 4 Write byte 1; EQADJA

ADDITIONAL GAIN POSITIONS (dB)	BITS OF DATA BYTE EQADJA							
	MSB							LSB
	NOT USED	NOT USED	EQA5	EQA4	EQA3	EQA2	EQA1	EQA0
0	0	0	0	0	0	0	0	0
0.4	0	0	0	0	0	0	0	1
0.8	0	0	0	0	0	0	1	0
1.2	0	0	0	0	0	0	1	1
1.6	0	0	0	0	0	1	0	0
2.0	0	0	0	0	0	1	0	1
2.4	0	0	0	0	0	1	1	0
2.8	0	0	0	0	0	1	1	1
3.2	0	0	0	0	1	0	0	0
3.6	0	0	0	0	1	0	0	1
4.0	0	0	0	0	1	0	1	0
4.4	0	0	0	0	1	0	1	1
4.8	0	0	0	0	1	1	0	0
5.2	0	0	0	0	1	1	0	1
5.6	0	0	0	0	1	1	1	0
6.0	0	0	0	0	1	1	1	1
6.4	0	0	0	1	0	0	0	0
6.8	0	0	0	1	0	0	0	1
7.2	0	0	0	1	0	0	1	0
7.6	0	0	0	1	0	0	1	1
8.0	0	0	0	1	0	1	0	0
8.4	0	0	0	1	0	1	0	1
8.8	0	0	0	1	0	1	1	0
9.2	0	0	0	1	0	1	1	1
9.6	0	0	0	1	1	0	0	0
10.0	0	0	0	1	1	0	0	1
10.4	0	0	0	1	1	0	1	0
10.8	0	0	0	1	1	0	1	1
11.2	0	0	0	1	1	1	0	0
11.6	0	0	0	1	1	1	0	1
12.0	0	0	0	1	1	1	1	0
12.4	0	0	0	1	1	1	1	1
12.8	0	0	1	0	0	0	0	0
13.2	0	0	1	0	0	0	0	1
13.6	0	0	1	0	0	0	1	0
14.0	0	0	1	0	0	0	1	1
14.4	0	0	1	0	0	1	0	0

ADDITIONAL GAIN POSITIONS (dB)	BITS OF DATA BYTE EQADJA							
	MSB							LSB
	NOT USED	NOT USED	EQA5	EQA4	EQA3	EQA2	EQA1	EQA0
14.8	0	0	1	0	0	1	0	1
15.2	0	0	1	0	0	1	1	0
15.6	0	0	1	0	0	1	1	1
16.0	0	0	1	0	1	0	0	0
16.4	0	0	1	0	1	0	0	1
16.8	0	0	1	0	1	0	1	0
17.2	0	0	1	0	1	0	1	1
17.6	0	0	1	0	1	1	0	0
18.0	0	0	1	0	1	1	0	1
18.4	0	0	1	0	1	1	1	0
18.8	0	0	1	0	1	1	1	1
19.2	0	0	1	1	0	0	0	0
19.6	0	0	1	1	0	0	0	1
20.0	0	0	1	1	0	0	1	0
20.4	0	0	1	1	0	0	1	1
20.8	0	0	1	1	0	1	0	0
21.2	0	0	1	1	0	1	0	1
21.6	0	0	1	1	0	1	1	0
22.0	0	0	1	1	0	1	1	1
22.4	0	0	1	1	1	0	0	0
22.8	0	0	1	1	1	0	0	1
23.2	0	0	1	1	1	0	1	0
23.6	0	0	1	1	1	0	1	1
24.0	0	0	1	1	1	1	0	0
24.4	0	0	1	1	1	1	0	1
24.8	0	0	1	1	1	1	1	0
25.2	0	0	1	1	1	1	1	1

Table 5 Write byte 2; EQADJB

ADDITIONAL GAIN POSITIONS (dB)	BITS OF DATA BYTE EQADJB							
	MSB							LSB
	NOT USED	NOT USED	EQB5	EQB4	EQB3	EQB2	EQB1	EQB0
0	0	0	0	0	0	0	0	0
0.4	0	0	0	0	0	0	0	1
0.8	0	0	0	0	0	0	1	0
1.2	0	0	0	0	0	0	1	1
1.6	0	0	0	0	0	1	0	0
2.0	0	0	0	0	0	1	0	1
2.4	0	0	0	0	0	1	1	0
2.8	0	0	0	0	0	1	1	1
3.2	0	0	0	0	1	0	0	0
3.6	0	0	0	0	1	0	0	1
4.0	0	0	0	0	1	0	1	0
4.4	0	0	0	0	1	0	1	1
4.8	0	0	0	0	1	1	0	0
5.2	0	0	0	0	1	1	0	1
5.6	0	0	0	0	1	1	1	0
6.0	0	0	0	0	1	1	1	1
6.4	0	0	0	1	0	0	0	0
6.8	0	0	0	1	0	0	0	1
7.2	0	0	0	1	0	0	1	0
7.6	0	0	0	1	0	0	1	1
8.0	0	0	0	1	0	1	0	0
8.4	0	0	0	1	0	1	0	1
8.8	0	0	0	1	0	1	1	0
9.2	0	0	0	1	0	1	1	1
9.6	0	0	0	1	1	0	0	0
10.0	0	0	0	1	1	0	0	1
10.4	0	0	0	1	1	0	1	0
10.8	0	0	0	1	1	0	1	1
11.2	0	0	0	1	1	1	0	0
11.6	0	0	0	1	1	1	0	1
12.0	0	0	0	1	1	1	1	0
12.4	0	0	0	1	1	1	1	1
12.8	0	0	1	0	0	0	0	0
13.2	0	0	1	0	0	0	0	1
13.6	0	0	1	0	0	0	1	0
14.0	0	0	1	0	0	0	1	1
14.4	0	0	1	0	0	1	0	0

ADDITIONAL GAIN POSITIONS (dB)	BITS OF DATA BYTE EQADJB							
	MSB							LSB
	NOT USED	NOT USED	EQB5	EQB4	EQB3	EQB2	EQB1	EQB0
14.8	0	0	1	0	0	1	0	1
15.2	0	0	1	0	0	1	1	0
15.6	0	0	1	0	0	1	1	1
16.0	0	0	1	0	1	0	0	0
16.4	0	0	1	0	1	0	0	1
16.8	0	0	1	0	1	0	1	0
17.2	0	0	1	0	1	0	1	1
17.6	0	0	1	0	1	1	0	0
18.0	0	0	1	0	1	1	0	1
18.4	0	0	1	0	1	1	1	0
18.8	0	0	1	0	1	1	1	1
19.2	0	0	1	1	0	0	0	0
19.6	0	0	1	1	0	0	0	1
20.0	0	0	1	1	0	0	1	0
20.4	0	0	1	1	0	0	1	1
20.8	0	0	1	1	0	1	0	0
21.2	0	0	1	1	0	1	0	1
21.6	0	0	1	1	0	1	1	0
22.0	0	0	1	1	0	1	1	1
22.4	0	0	1	1	1	0	0	0
22.8	0	0	1	1	1	0	0	1
23.2	0	0	1	1	1	0	1	0
23.6	0	0	1	1	1	0	1	1
24.0	0	0	1	1	1	1	0	0
24.4	0	0	1	1	1	1	0	1
24.8	0	0	1	1	1	1	1	0
25.2	0	0	1	1	1	1	1	1

Table 6 Write byte 3; OFFCHA

OFFSET CHANNEL A POSITIONS	BITS OF DATA BYTE OFFCHA							
	MSB							LSB
	OFA7	OFA6	OFA5	OFA4	OFA3	OFA2	OFA1	OFA0
Maximum positive	0	0	0	0	0	0	0	0
	...	...	...	...	...	...	...	...
Maximum negative	1	1	1	1	1	1	1	1

Table 7 Write byte 4; OFFCHB

OFFSET CHANNEL B POSITIONS	BITS OF DATA BYTE OFFCHB							
	MSB							LSB
	OFB7	OFB6	OFB5	OFB4	OFB3	OFB2	OFB1	OFB0
Maximum positive	0	0	0	0	0	0	0	0
	...	...	...	...	...	...	...	...
Maximum negative	1	1	1	1	1	1	1	1

Table 8 Optionally pin controlled switch functions

FUNCTIONS	HS (PIN 18)			EQS (PIN 5)		
	PIN STATE		DATA BIT HSW	PIN STATE		DATA BIT EQT
	OUTPUT	INPUT		OUTPUT	INPUT	
Equalization time constant						
70 µs	–	–	–	LOW	open-circuit	0
120 µs	–	–	–	HIGH	open-circuit	1
70 µs	–	–	–	LOW	LOW	–
Head switch						
IN2	LOW	open-circuit	0	–	–	–
IN1	HIGH	open-circuit	1	–	–	–
IN2	LOW	LOW	–	–	–	–

Table 9 MAD switch

MODULE ADDRESS	MAD (PIN 1)
101 100 10	open-circuit
101 100 10	HIGH
101 100 00	LOW

Table 10 BEN switch

I²C-BUS OPERATION MODE	BEN (PIN 32)
Active; 5 V thresholds	open-circuit
Active; 5 V thresholds	HIGH (5 V to V_{CC})
Active; V_{BEN} related thresholds	HIGH (3 to 5 V)
Inactive	LOW

I²C-bus transmission types

The I²C-bus format depends on the kind of data which should be transmitted. To speed up the offset adjustment procedure three types of transmissions from master to slave are possible. The transmission type is controlled by bits OFCH and OMOR in write byte 0.

If the OMOR bit is set to logic 0 the standard transmission type is used. The corresponding byte sequence is shown in Fig.13. This kind of transmission should by used for changes in the IC settings during normal operation.

If the OMOR bit is set to logic 1 and the OFCH bit is set to logic 0 the transmission type for an offset adjust in channel A is selected. The byte sequence is shown in Fig.14. During this kind of transmission the pin AMS is used as the offset monitor output for channel A.

If the OMOR bit is set to logic 1 and the OFCH bit is set to logic 1 the transmission type for an offset adjust in channel B is selected. The byte sequence is shown in Fig.15. During this kind of transmission the pin AMS is used as the offset monitor output for channel B.

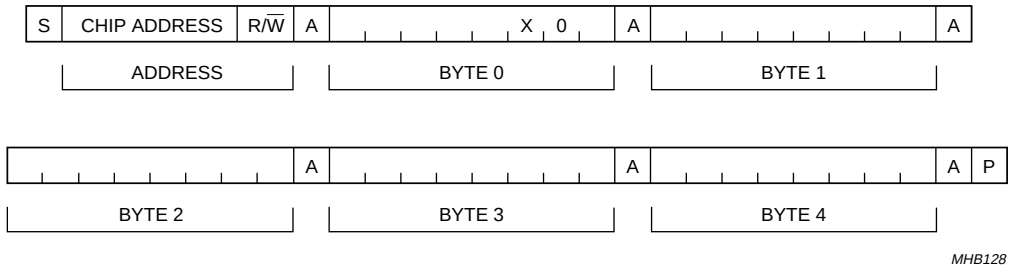


Fig.13 Standard transmission.

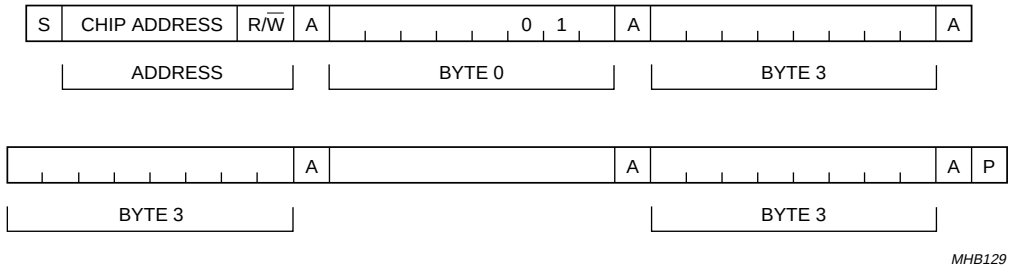


Fig.14 Offset adjust channel A transmission.

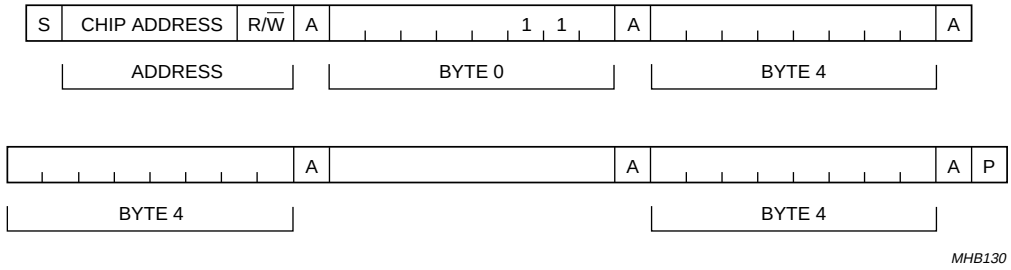


Fig.15 Offset adjust channel B transmission.

INTERNAL PIN CONFIGURATIONS

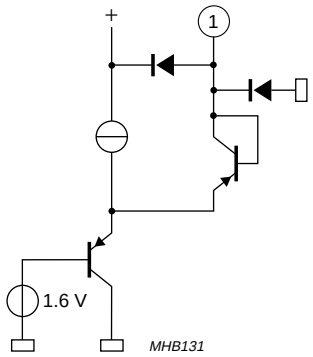


Fig.16 Pin 1: programmable address bit.

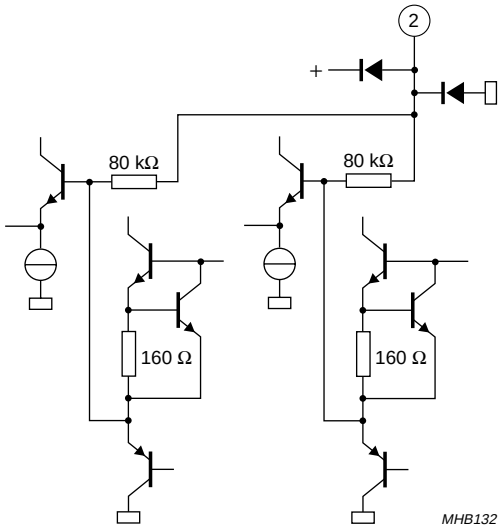


Fig.17 Pin 2: blank skip reference capacitance.

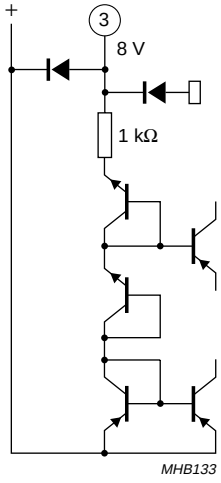


Fig.18 Pin 3: delay time constant.

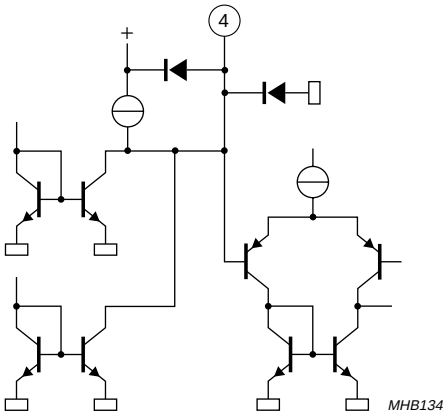


Fig.19 Pin 4: blank skip integration capacitance.

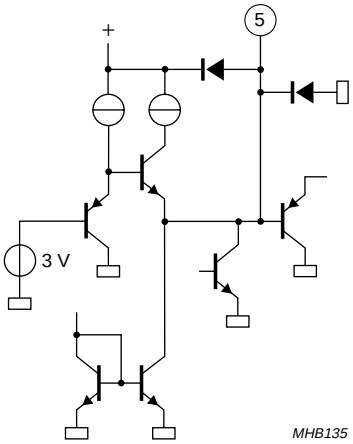


Fig.20 Pin 5: EQ switch input.

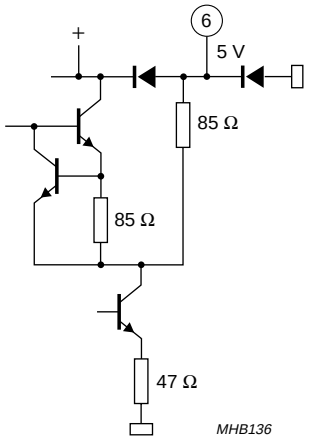


Fig.21 Pins 6 and 27: output channel.

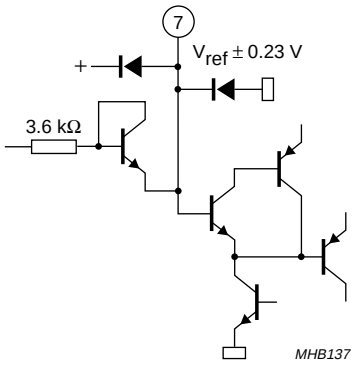


Fig.22 Pin 7: integrating filter channel A.

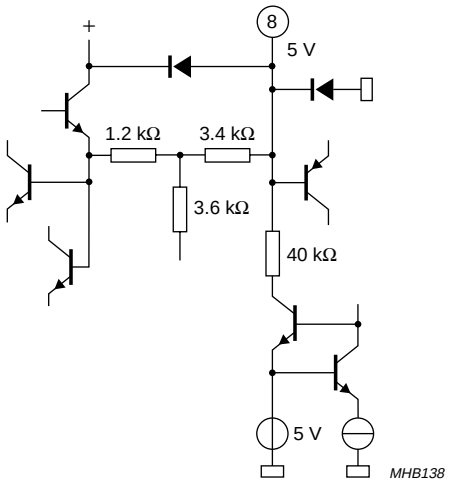


Fig.23 Pin 8: control voltage channel A.

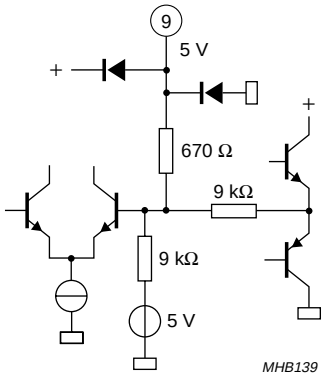


Fig.24 Pins 9 and 24: high-pass filter.

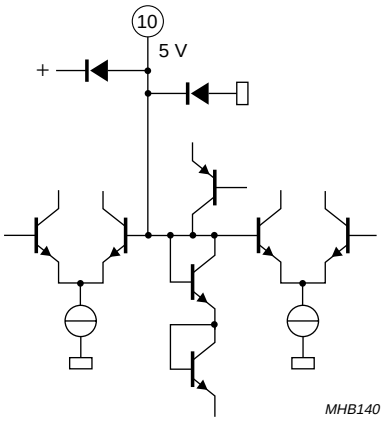


Fig.25 Pins 10 and 23: side chain.

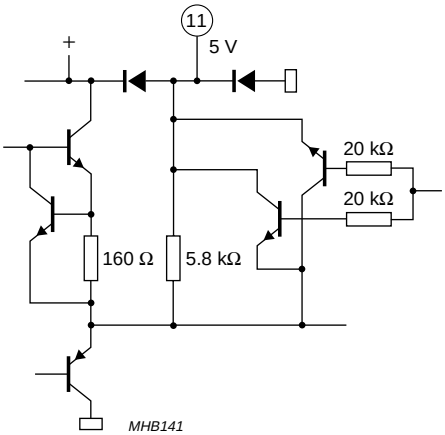


Fig.26 Pins 11 and 22: equalizing output.

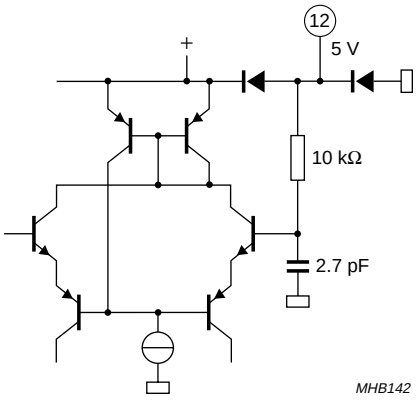


Fig.27 Pins 12 and 21: equalizing input.

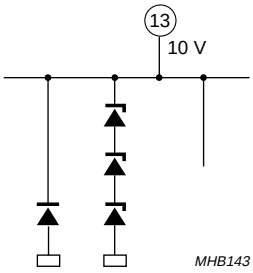


Fig.28 Pin 13: supply voltage.

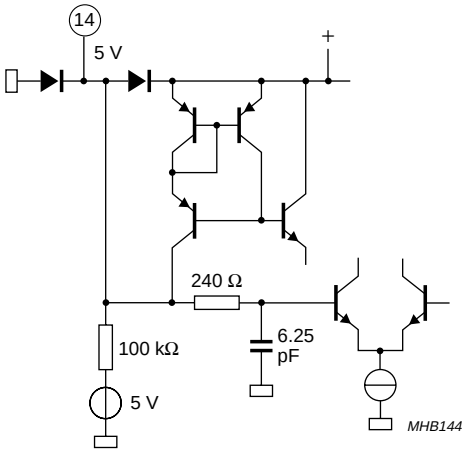


Fig.29 Pins 14, 16, 17 and 19: input channel.

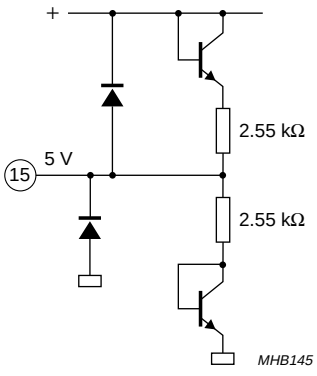


Fig.30 Pin 15: reference voltage.

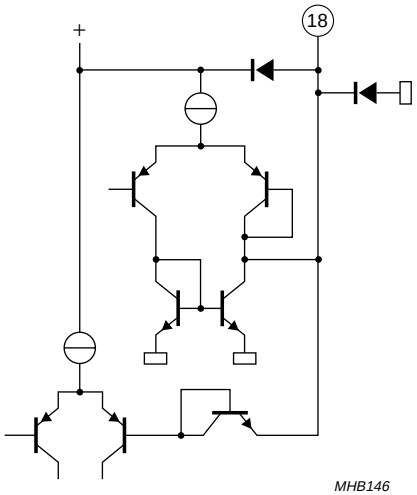


Fig.31 Pin 18: head switch input.

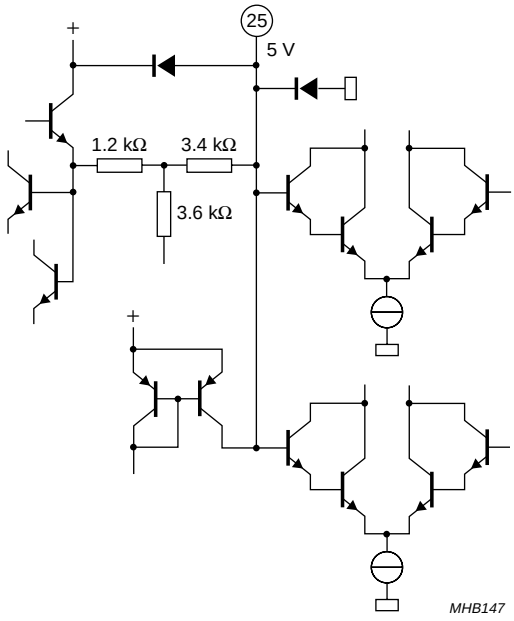


Fig.32 Pin 25: control voltage channel B.

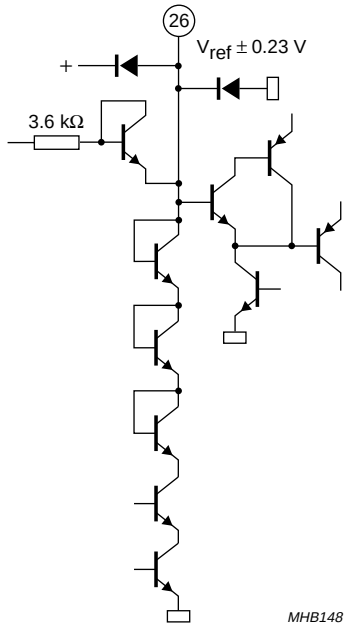


Fig.33 Pin 26: integrating filter channel B.

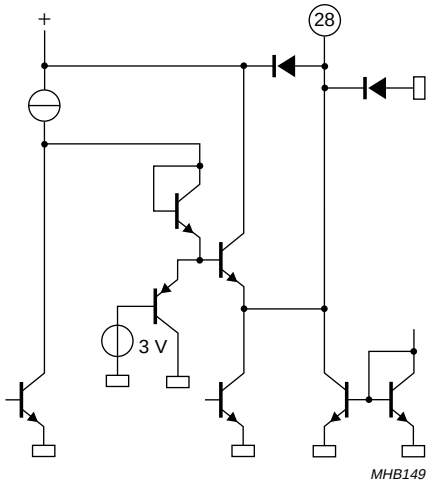


Fig.34 Pin 28: AMS output.

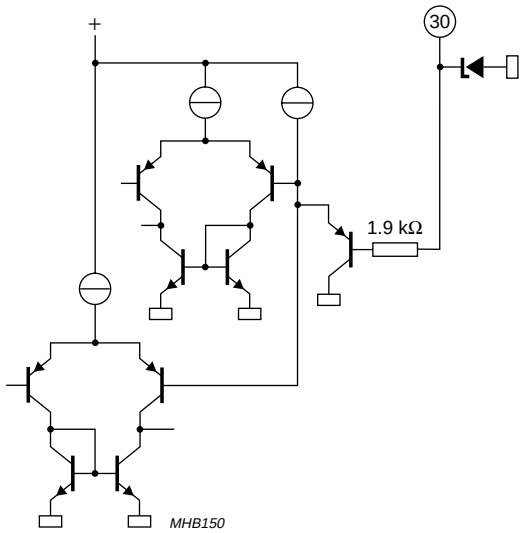


Fig.35 Pin 30: serial clock input.

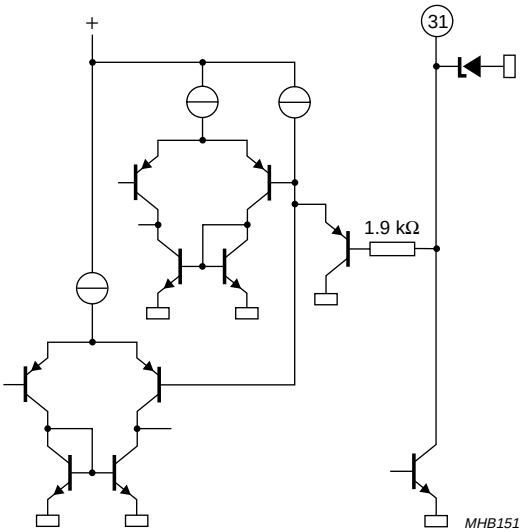


Fig.36 Pin 31: serial data input/output.

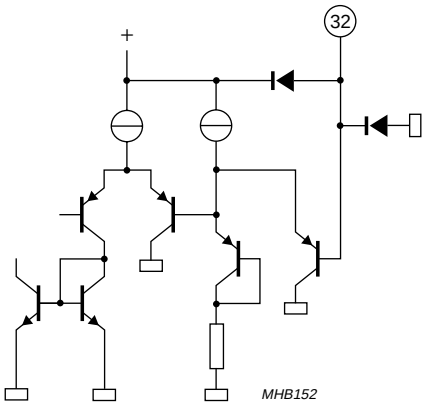


Fig.37 Pin 32: bus enable.

TEST AND APPLICATION INFORMATION

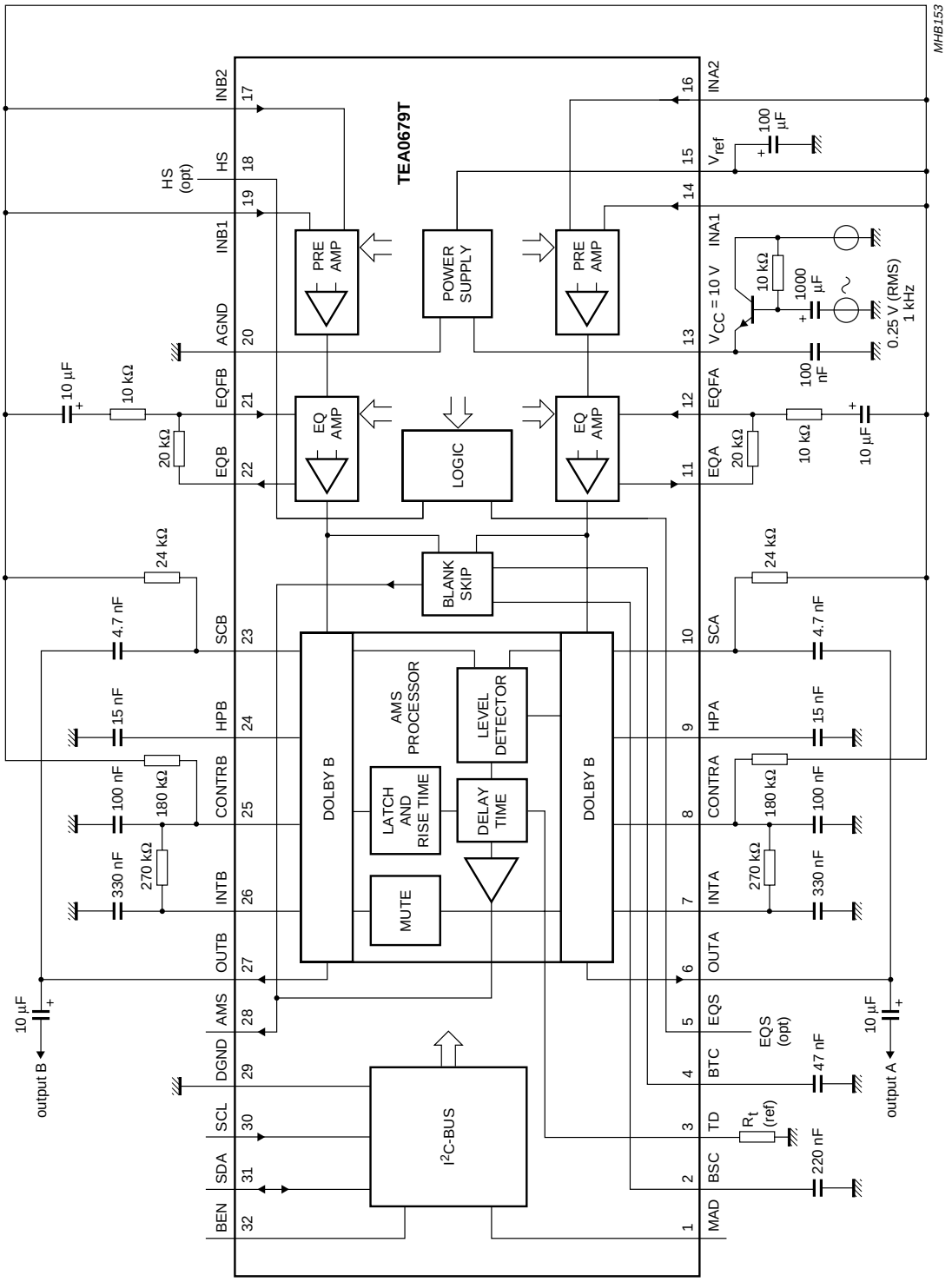


Fig.38 Test circuit for power supply ripple rejection.

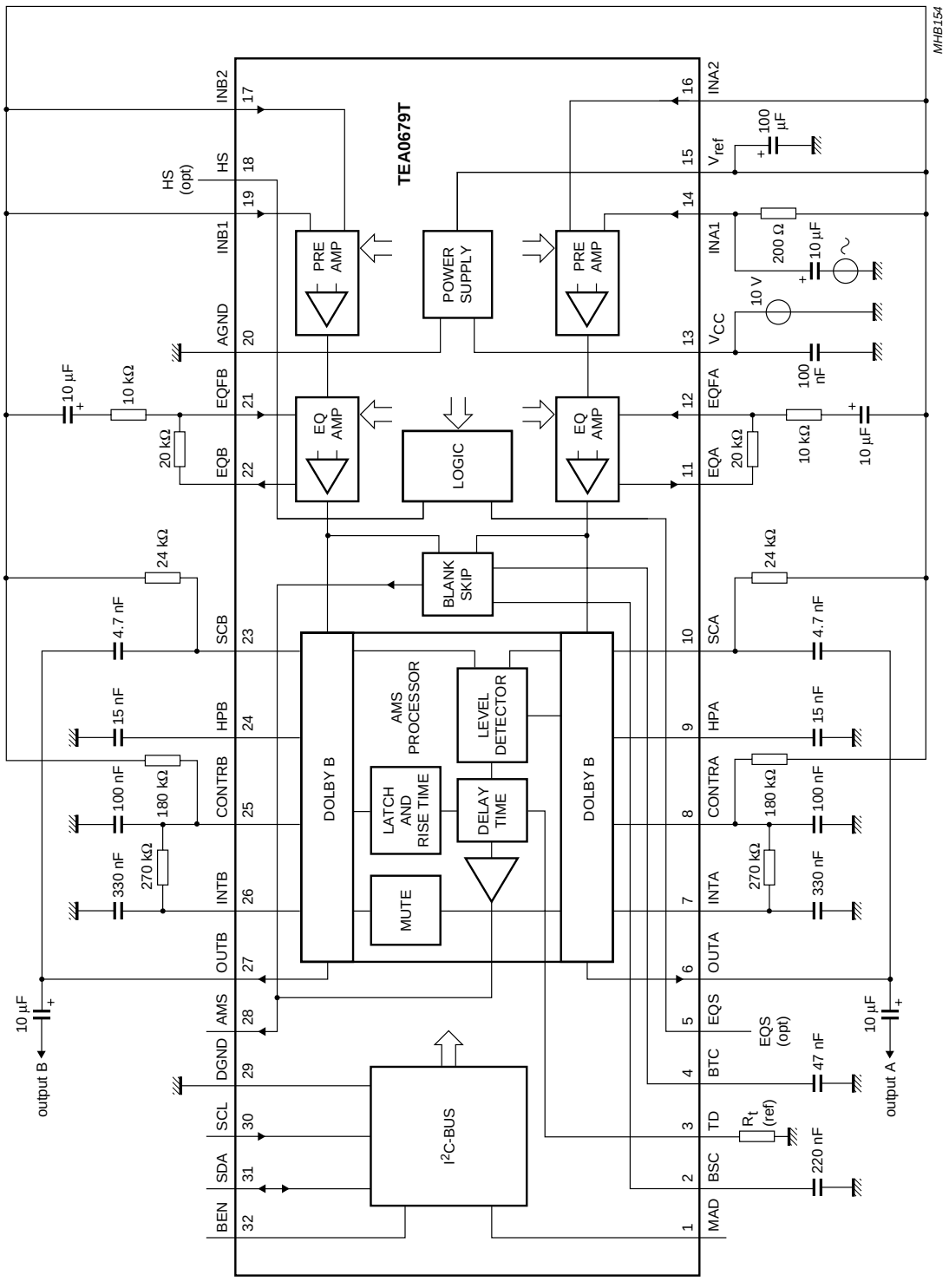


Fig.39 Test circuit for channel separation.

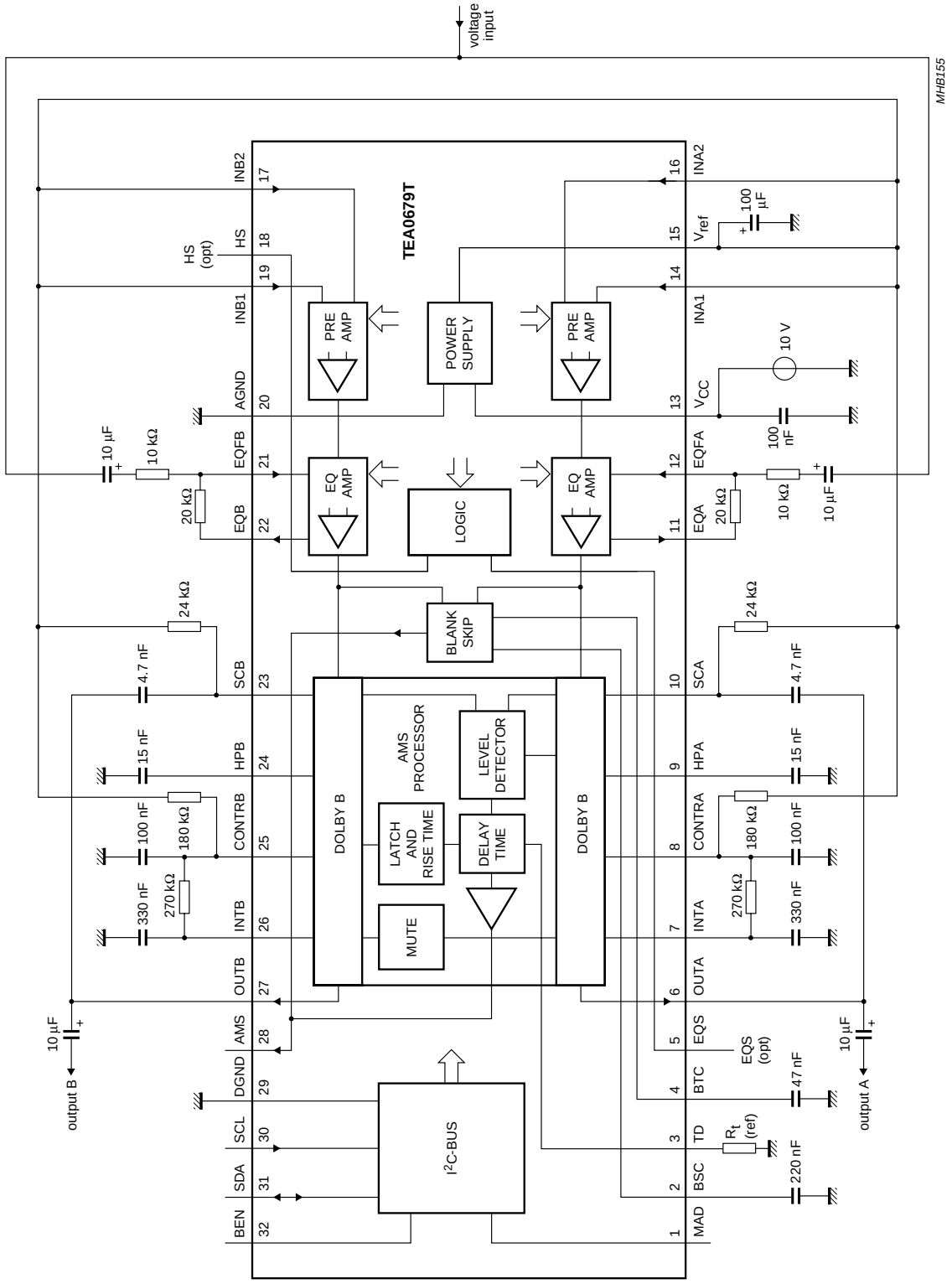
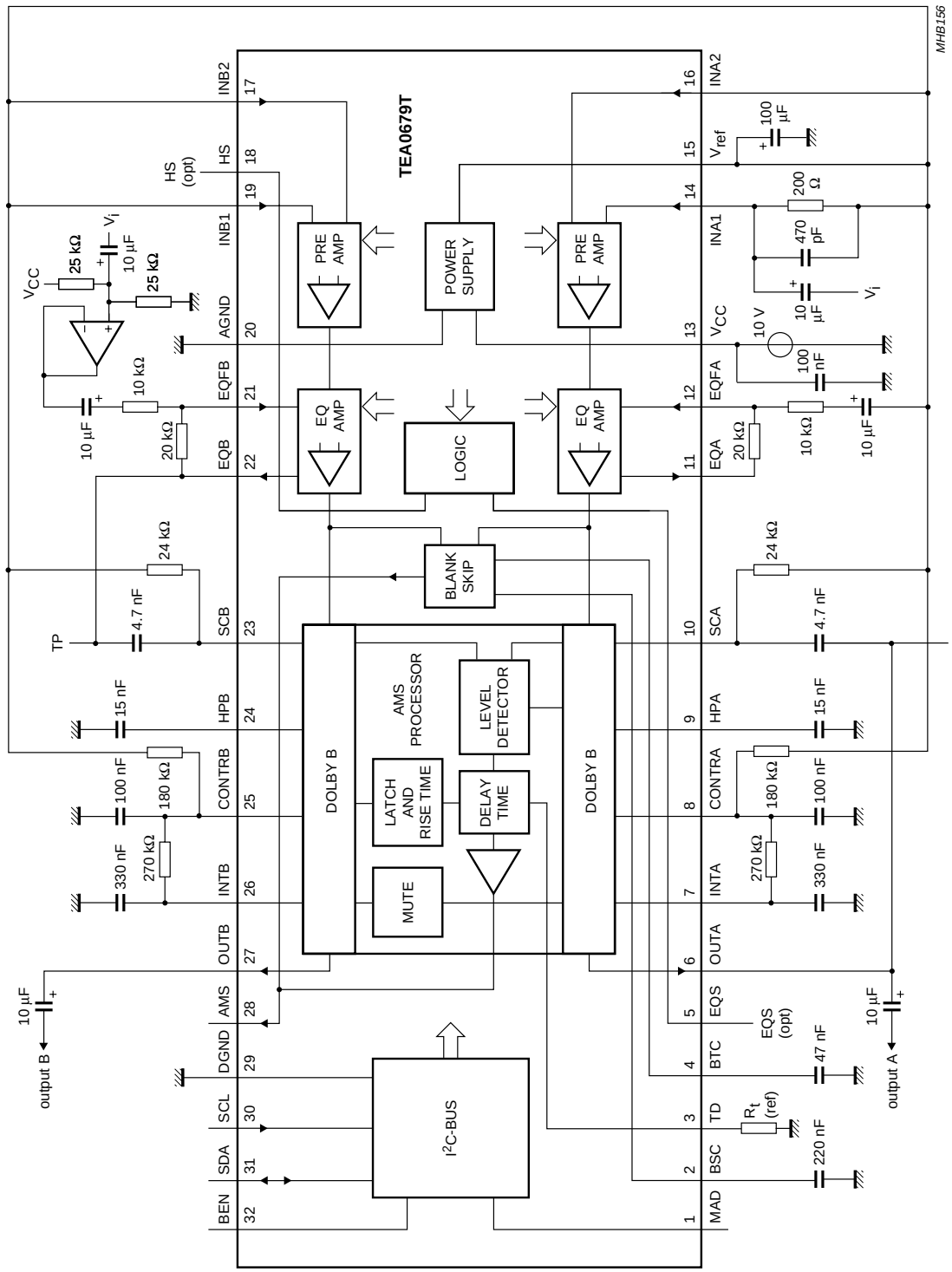


Fig.40 Test circuit for AMS threshold level.



Channel A: Decode mode: pre-amplifier 30 dB and EQ amplifier 10 dB linear.
Channel B: Encode mode.

Fig.41 Test circuit for frequency response (channel B).

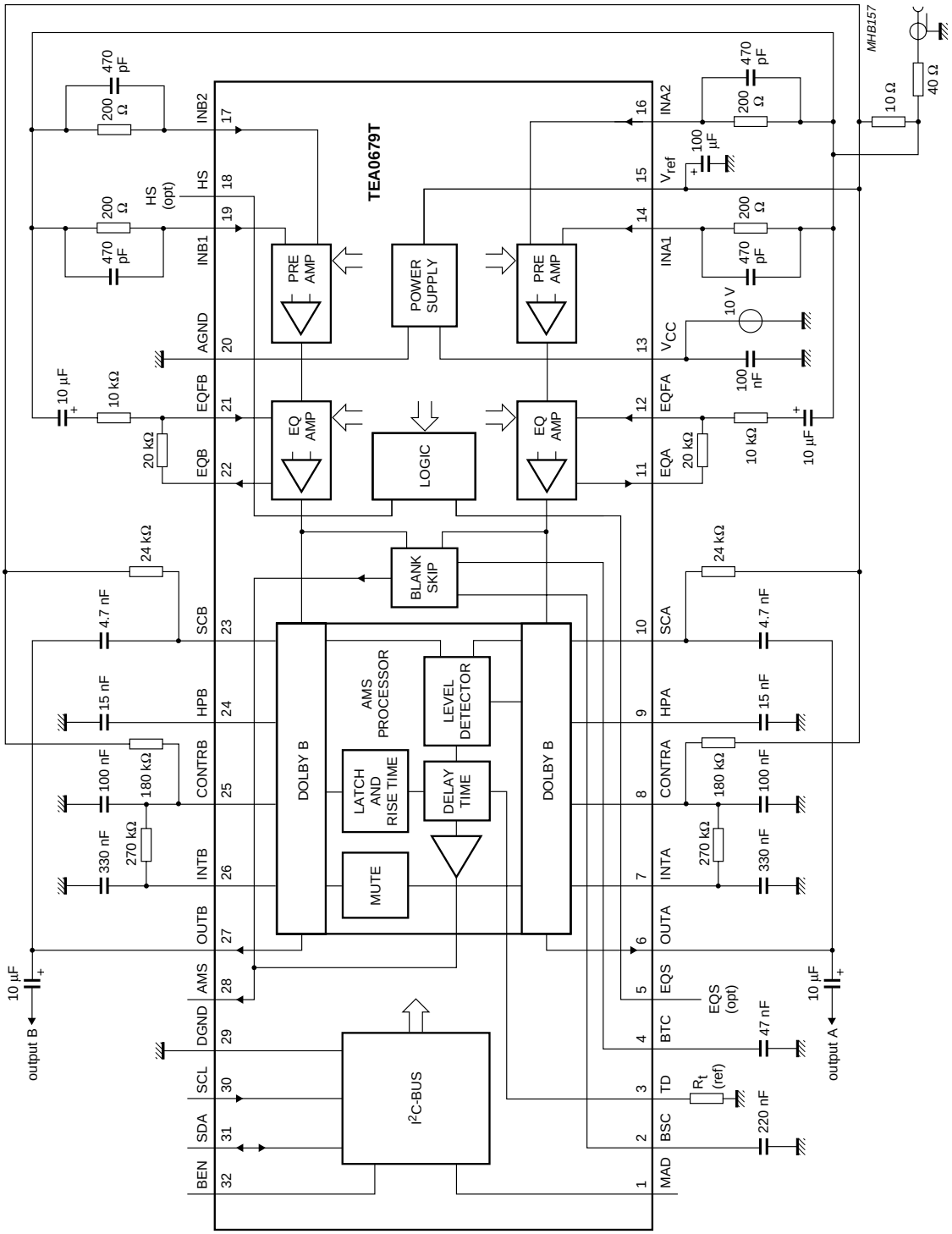
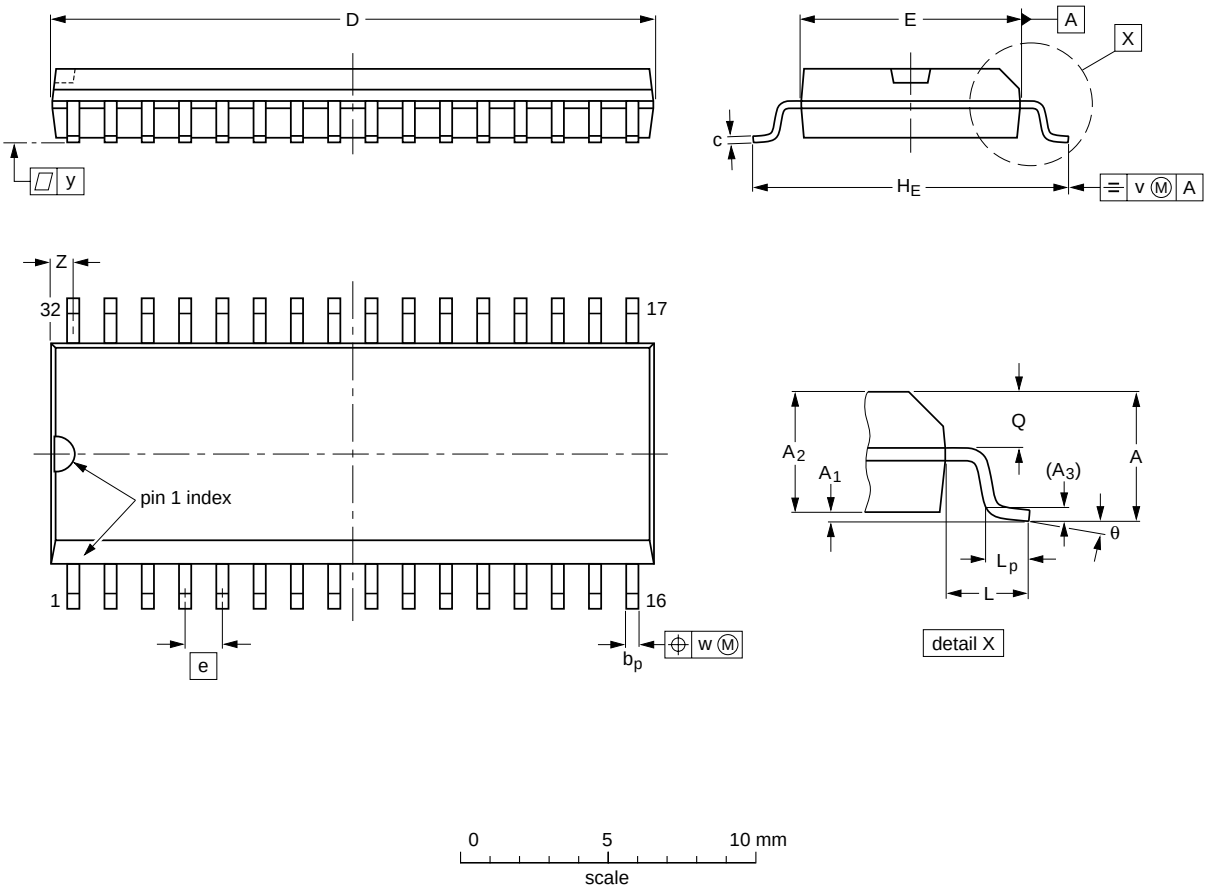


Fig.42 EMC test circuit.

PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~95-01-25~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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